Method and Apparatus for Prioritized Instruction Issue Queue

ABSTRACT OF THE INVENTION

An apparatus and method in a high performance processor for issuing instructions, comprising; a classification logic for sorting instructions in a number of priority categories, a plurality of instruction queues storing the instruction of differing priorities, and a issue logic selecting from which queue to dispatch instructions for execution. This apparatus and method can be implemented in both in-order, and out-of-order execution processor architectures. The invention also involves instruction cloning, and use of various predictive techniques.